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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/050,160	01/18/2002	Masatsugu Kitada	04329.2724	7613

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 06/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/050,160	KITADA ET AL.	
	Examiner	Art Unit	
	James C Kerveros	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-11* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/18/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The specification is objected to under 37 CFR 1.71 because it lacks an enabling description for claim 7, in reference to the limitation real measuring time $\Delta t \times i$.

Appropriate correction is required.

Claim Objections

Claims 1-11 are objected to because of the following informalities: Appropriate correction is required.

Claims 1-11 require indentation. Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation. There may be plural indentations to further segregate subcombinations or related steps. See 37 CFR 1.75 and MPEP § 608.01(m).

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 7 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not

described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The specification, page 16, lines 1-5, fails to clearly describe the equation for the "real measuring time" recited in claim 7.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1, 3, 5 and 8-10, the phrase "such" recited throughout the main body of the claims renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention.

Also, in claim 1, the limitation "in a manner" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Claim 7 is indefinite because the limitation "by one real measuring time .DELTA.t.times.i." fails to clearly define the mathematical expression of the claimed equation.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5 and 7 -11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto (US 6263463).

Regarding independent Claims 1, 3, 5 and 9-11, Hashimoto substantially discloses a semiconductor test system and method for providing test signals to the semiconductor device under test and comparing the resulting output of the device under test with expected data to determine whether the semiconductor device (DUT) works correctly or not, FIG. 1, comprising:

A test program memory section (FIG. 1), which includes a pattern generator 31, a timing generator 32, and wait time variable delay circuits 12, 13a and 13b, for testing the semiconductor device.

A measuring/deciding section, including such as a wave formatter 33 which generates a test signal which is used for the purpose of adjusting the timings in the test stations ST1 and ST2, and then after the timing adjustment, the wave formatter 33 provides an actual test signal to the semiconductor devices DUT (a) and DUT (b) to be tested mounted on the test stations ST1 and ST2.

Detecting an optimal value of the wait time using detection circuit 15 which receives the test signals returned from the test stations ST1 and ST2 to detect the changes of the logic comparator outputs (38a and 38b), by measuring the electrical

characteristics of the semiconductor device, and comparing the resulting output of the device under test with expected data form pattern generator 31 to determine whether the semiconductor device works correctly or not corresponding to an OK/NG decision.

If the decision is "NG", such that if the test stations ST1 and ST2 signals are not synchronized, prior to the test of DUT, the timings of the test stations ST1 and ST2 are adjusted automatically by the variable delay circuit 12, 13a and 13b and the timing control circuit 8, which detects the outputs of the analog comparators 36a and 36b and automatically sets the delay time of the variable delay circuit 12, 13a and 13b and consequently performing the adjustment operation on the electrical characteristics of the semiconductor device until the result of such a decision is "OK", namely ST1 and ST2 signals are synchronized and initiating the next measuring operation when the result of that decision is "OK".

Repeat the setting of the wait time until the result of the decision is "OK", when both the two test signals to the comparator change their states at the same time, it means that the timing phases are adjusted to be the same, and the timing phase adjustment process ends by holding all the delay data at that time to fix the delay time in the variable delay circuits 12, 13a and 13b. Then, an actual test starts in parallel for the plurality of semiconductor devices placed on the test stations.

Regarding independent Claims 1, 3, 9, 10, Hashimoto does not explicitly disclose detecting an optimal value of the wait time through a series of processes including measuring, after elapse of the wait time, the electrical characteristics of the semiconductor device on the basis of the response signal outputted from the

semiconductor device. However, Hashimoto discloses a timing phase adjustment circuit for adjusting the timings of the input signals to the test stations ST1 and ST2, prior to DUT testing and also an actual test signal to the semiconductor devices DUT to be tested. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the adjustment circuit, as taught by Hashimoto, to perform timing adjustments of the output response signals from the semiconductor device DUT, since the input signals being adjusted and the output response signals share the same hardware, such as detection circuit (15) and logic comparators (38a and 38b), for comparing the resulting output of the device under test with expected data form pattern generator 31 to determine whether the semiconductor device works correctly or not.

Regarding independent Claims 5 and 11, Hashimoto does not explicitly disclose a measuring processing loop for performing measurements in a repeated way, storing the results of such measurements, counting the number of measurements, i, where i=a positive integer of 1 or more, if it is decided that the number of measurements, i, equals a target number of measurements, j, where j=a positive integer of 1 or more, analyzing in real time based on a statistical procedure a data array corresponding to a j number of measurement results obtained by the number of measurements, j, deciding a stable state of the measuring data from the result of analysis, if the result of the decision is found to be "NG", then repeating such measurement for automatically detecting the optimal wait time value.

However, Hashimoto provides a timing phase adjustment circuit for a semiconductor test system for automatically adjusting timing differences between a plurality of test stations for testing a plurality of semiconductor devices. The timing phase adjustment circuit automatically sets the delay time of the variable delay circuit 12, 13a and 13b and consequently performs the adjustment operation on the electrical characteristics of the semiconductor device until the result of such a decision is "OK", namely ST1 and ST2 signals are synchronized and then initiates the next measuring operation when the result of that decision is "OK". Furthermore, it is not inventive to discover the optimum or workable ranges by routine experimentation, such as in this case performing measurements on a semiconductor device in a repeated way for obtaining an optimal value, "in re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)". It would have been obvious to a person having ordinary skill in the art at the time the invention was made to perform routine experimentation, as taught by the cited case of Aller, using Hashimoto's timing phase adjustment circuit, for the purpose of adjusting the timing differences between a plurality of test stations, so as to ensure the proper operation of a semiconductor device under test.

Regarding Claims 2, 4 and 8, Hashimoto discloses a first memory section, registers G and H in the delay data hold control circuit (17) for storing the result of the OK/NG decision from the detection circuit 15 as a flag and a second memory section, latches J and K of the delay data hold circuit (16) for storing the wait time.

Regarding Claim 7, as best understood, Hashimoto substantially discloses wait time calculating device, such as latches J and K of the delay data hold circuit (16) for

storing the wait time. Hashimoto does not explicitly disclose an equation $\Delta t \times i$ for calculating the real measuring time. Further, Hashimoto discloses a timing phase adjustment circuit (FIG. 2) including a counter 10 which increments its output by one in synchronism with the system clock for controlling the delay data hold circuit 16. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement a counter with a delay data hold circuit, as taught by Hashimoto, for the purpose of measuring a delay time, since a counter is ideal for generating synchronized data with a system clock.

Allowable Subject Matter

Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior arts of record taken alone or in combination fail to teach, anticipate, suggest or render obvious the claimed invention for a calculating device, connected to the measuring data memory device and number of measurements deciding device, for calculating based on a statistical procedure a data array corresponding to the j number of measurement results obtained from the number of measurements, j, and analyzing the measured data in real time, and a stable state deciding device, connected to the calculation device, for deciding a stable state of the measured data from the analytical result of the calculation device, the measuring processing loop being a series of

repeated processes for, if a result of stable state decision is found to be "NG", effecting the measurements, real time analysis on a new data array based on the statistical procedure and stable state decision.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
Email: james.kerveros@uspto.gov

Date: 25 May 2004
Office Action: Non-Final Rejection

By: _____

James C Kerveros
Examiner
Art Unit 2133

Gary J. Lamarre
for

Albert DeCady
Primary Examiner